## Claims

What is claimed:

1. An Ethernet transceiver comprising:

    a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

    a domain transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a lower complexity domain;

    a processor for joint processing of the transformed sub-blocks of the digital signal streams, each joint processed digital signal stream sub-block being influenced by other digital signal streams sub-blocks; and

    an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.

2. The transceiver of claim 1, wherein a sub-block includes less digital signal stream samples than a block, wherein a block includes enough digital signal stream samples that transforming and processing blocks of the digital signal streams does not introduce distortion.

3. The transceiver of claim 1, wherein a sub-block includes less digital signal stream samples than a block, wherein a block includes enough samples to exceed the joint filter time sample spans of the digital signal streams.

4. The transceiver of claim 1, wherein same size sub-blocks are used for transmit and receive joint processing.

5. The transceiver of claim 1, wherein the domain transformer uses common sub-block transformers for both transmit and receive joint processing.

6. The transceiver of claim 1, wherein an accuracy of each joint sub-block is dependent upon a magnitude of the coupling.

7. The transceiver of claim 1, wherein the joint processing comprises sub-block filters, and a subset of the sub-block filters are disabled when the coupling is below a threshold.

8. The transceiver of claim 1, wherein the joint processing includes multiplying each of the digital signal streams sub-blocks with sub-block processing matrices.

9. The transceiver of claim 8, wherein diagonal elements of the sub-block processing matrices are selected to reduce inter-symbol interference of the digital signal streams.

10. The transceiver of claim 9, wherein diagonal elements of the sub-block processing matrices are adaptively selected.

11. The transceiver of claim 10 wherein diagonal elements of the sub-block processing matrices are adaptively selected depending upon signal coupling and inter-symbol interference measurements.

12. The transceiver of claim 8, wherein off-diagonal elements of the sub-block processing matrices are selected to reduce cross-talk between the digital signal streams.

13. The transceiver of claim 12, wherein the off-diagonal elements of the sub-block processing matrices are adaptively selected.

14. The transceiver of claim 13, wherein off-diagonal elements of the sub-block processing matrices are adaptively selected depending upon signal coupling and inter-symbol interference measurements.

15. The transceiver of claim 8, wherein the transceiver is transmitting the digital signal streams, and the off-diagonal elements of the sub-block processing matrices are selected to provide process cross-talk between the digital signal streams, which cancel transmission cross-talk of the digital signal streams introduced during transmission of the digital signal streams.

16. The transceiver of claim 8, wherein the transceiver is receiving the digital signal streams, and the off-diagonal elements of the sub-block processing matrices are selected to cancel transmission cross-talk of the digital signal streams introduced during transmission of the digital signal streams.

17. The transceiver of claim 8, wherein the transceiver is receiving the digital signal streams, and the diagonal elements of the sub-block processing matrices are selected to cancel transmission cross-talk of the digital signal streams introduced during reception of the digital signal streams.

18. The transceiver of claim 1, wherein at least one digital signal stream includes time domain processing.

19. The transceiver of claim 1, wherein the joint processing of the transformed signal streams is performed on signal streams to be transmitted.

20. The transceiver of claim 1, wherein the joint processing of the transformed signal streams is performed on received signal streams.

21. The transceiver of claim 1, including N digital signal streams, and M joint processed signal streams.

22. The transceiver of claim 1, including N digital signal streams, and a single joint processed signal stream.

23. The transceiver of claim 1, wherein the transform block additionally transforms filtering coefficients.

24. The transceiver of claim 1, wherein filtering coefficients of the joint processing are determined to reduce interference between Ethernet digital signal streams.

25. The transceiver of claim 24, wherein the filtering coefficients include a transfer domain representation of a time domain filter.

26. The transceiver of claim 1, wherein the digital signal streams are transmitted over an Ethernet network.

27. The transceiver of claim 1, wherein the joint processing provides reduction of near end cross talk.

28. The transceiver of claim 1, wherein the joint processing provides reduction of alien near end cross talk.

29. The transceiver of claim 1, wherein the joint processing provides reduction of far end cross talk.

30. The transceiver of claim 1, wherein the joint processing provides reduction of echo signal interference.

31. The transceiver of claim 1, wherein the joint processing provides reduction of inter-symbol interference.

32. A transceiver comprising:

a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a new domain that allows for less complex processing;

a processor for joint processing the transformed sub-blocks of the digital signal streams in the new domain, each joint processed digital signal stream sub-block being influenced by other digital signal stream sub-blocks;

an inverse transform block for inverse transforming the joint processed signal stream sub-blocks back to the original domain.

33. A transmitter comprising:

a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a new domain that allows for less complex processing;

a processor for joint processing the transformed sub-blocks of the digital signal streams in the new domain, each joint processed digital signal stream sub-block being influenced by other digital signal stream sub-blocks;

an inverse transform block for inverse transforming the joint processed signal stream sub-blocks back to the original domain; and

an analog front end for transmitting the joint processed signal streams.

34. A receiver comprising:

an analog front end for receiving analog signal streams, and generating a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a new domain that allows for less complex processing;

a processor for joint processing the transformed sub-blocks of the digital signal streams in the new domain, each joint processed digital signal stream sub-block being influenced by other digital signal stream sub-blocks;

an inverse transform block for inverse transforming the joint processed signal stream sub-blocks back to the original domain.

35. A method of joint processing a plurality of digital signal streams;

transforming a plurality of the digital signal streams from an original domain into a lower complexity processing domain;

joint processing of the transformed sub-blocks of the digital signal streams, each joint processed digital signal stream sub-block being influenced by characteristics of other digital signal stream sub-blocks;

inverse transforming the joint processed signal stream sub-blocks back to the original domain.

36. The method of claim 35, wherein same size sub-blocks are used for transmit and receive joint processing.

37. The method of claim 35, wherein the transforming uses common sub-block transformers for both transmit and receive joint processing.

38. The method of claim 35, wherein an accuracy of each joint sub-block is dependent upon a magnitude of the coupling.

39. The method of claim 35, wherein the joint processing comprises sub-block filters, and a subset of the sub-block filters are disabled when the coupling is below a threshold.

40. The method of joint processing of claim 35, wherein transforming additionally includes transforming filtering coefficients.

41. The method of joint processing of claim 35, wherein a maximal amount of Ethernet signal interference minimization processing is performed in the lower complexity domain.

42. The method of joint processing of claim 35, wherein filtering coefficients of the joint processing are determined to minimize interference between Ethernet digital signal streams.

43. The method of joint processing of claim 35, wherein the digital signal streams are transmitted over an Ethernet network.

44. The method of joint processing of claim 35, wherein the joint processing provides reduction of near end cross talk.

45. The method of joint processing of claim 35, wherein the joint processing provides reduction of alien near end cross talk.

46. The method of joint processing of claim 35, wherein the joint processing provides reduction of far end cross talk.

47. The method of joint processing of claim 35, wherein the joint processing provides reduction of inter-symbol interference.

48. The method of joint processing of claim 35, wherein the joint processing provides reduction of echo signal interference.

49. A network line card, the network line card comprising a bi-directional transceiver, the bi-directional transceiver comprising:

a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a domain transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a lower complexity domain;

a processor for joint processing of the transformed sub-blocks of the digital signal streams, each joint processed digital signal stream sub-block being influenced by other digital signal streams sub-blocks; and

an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.

50. A server comprising a bi-directional transceiver, the bi-directional transceiver comprising:

a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a domain transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a lower complexity domain;

a processor for joint processing of the transformed sub-blocks of the digital signal streams, each joint processed digital signal stream sub-block being influenced by other digital signal streams sub-blocks; and

an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.

51. A switch comprising a bi-directional transceiver, the bi-directional transceiver comprising:

a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a domain transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a lower complexity domain;

a processor for joint processing of the transformed sub-blocks of the digital signal streams, each joint processed digital signal stream sub-block being influenced by other digital signal streams sub-blocks; and

an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.

52. A LAN system comprising a bi-directional transceiver, the bi-directional transceiver comprising:

a plurality of digital signal streams, at least one digital signal stream being coupled to another of the digital signal streams;

a domain transformer for transforming sub-blocks of each of the plurality of the digital signal streams from an original domain into a lower complexity domain;

a processor for joint processing of the transformed sub-blocks of the digital signal streams, each joint processed digital signal stream sub-block being influenced by other digital signal streams sub-blocks; and

an inverse transformer for inverse transforming the joint processed signal streams sub-blocks back to the original domain.